SRC’s explicitly controlled processor is called MAP®
SRC Milestones

- First SRC system with MAP® installed at ORNL in 1999
  - Direct Execution Logic had merit
  - Needs tightly integrated programming environment

- First SRC-6E installed at GWU in 2002
  - Included Carte™ Programming Environment

- First SRC-6 with Hi-Bar® switch and Common Memory installed May 2004

- First MAPstation™ workstation delivered in Aug 2004

- First Portable MAPstation delivered in April 2005 to AFRL
Series E MAP®

- Control circuits allow explicit control of memory prefetch and data access
- Multiple banks of On-Board Memory maximizes local memory bandwidth
- Direct Execution Logic (DEL) made up of one or more User Logic device
- GPIO ports allow direct MAP to MAP chain connections or direct data input
- Multiple DMA engines support
  - Distributed SRAM in User Logic
    - 344 KBytes @ 1102 GB/s
  - Block SRAM in User Logic
    - 8 MBytes @ 355 GB/s
  - On-Board SRAM
    - 28 MB @ 9.6 GB/s
  - Microprocessor Memory
    - 6 GB/µP @ 1400 MB/s
  - Common Memory
    - 8 GB/bank, 2 TB max @ 1400 MB/s

MAP

- Dual-ported Memory (4 MB)
- User Logic 1
  - 30 Mgates
- User Logic 2
  - 30 Mgates

Controller

Six Banks Dual-ported On-Board Memory (24 MB)

1400 MB/s sustained payload each

4800 MB/s

4800 MB/s

4800 MB/s

2400 MB/s each

GPIO
Ease of Use

• Standard programming languages
  – C and Fortran used today
  – Additional languages driven by demand

• Standard operating system
  – Linux

• Systems run all legacy codes
  – IA microprocessors are integral to system

• Simple site integration
  – All standard server network interfaces available
Support for Development Process

• **Application Debug Environment**
  – Fast compile times
  – Familiar debugger environment
  – Debugging includes data movement to/from MAP®
  – Does not require MAP hardware to run
  – Fast enough to test a full application

• **Execution on MAP Hardware**
  – Compilation for MAP on the order 10s of minutes
  – Results match debug and simulation

• **Easy integration of Existing Direct Execution Logic**
  – Custom functional unit development supported
  – Functional unit simulation environment supported
SRC MAPstation™ with Hi-Bar®

*MAPstation towers hold up to 3 MAP or memory nodes*

MAPstation with 2 MAPs and Common Memory

MAPstation Configurations

MAPstation with 3 MAPs and Common Memory

**SRC Hi-Bar® Switch**

**MAP®**

**MEMORY**

**MAP®**

**GPIO Ports**

**SNAP™**

**Memory**

**µP**

**PCI-X/EXP**

**Disk**

**Storage Area Network**

**Local Area Network**

**Wide Area Network**

**Tower 2U**
SRC Hi-Bar® Based Systems

- Hi-Bar sustains 1.4 GB/s payload per port with 180 ns latency per tier
- Up to 256 input and 256 output ports with two tiers of switch
- Allow communication between any two nodes
- CM Controller can perform other functions such as scatter/gather
- GPIO supports both chain connections and direct sensor input
MAP Capacity Summary

60 Mgates

28 MB

2.4 GB/s

4.8 GB/s

5 /us

28 MB

9.6 GF

6.4 Gbytes/s

User Logic Size

Total Local Memory

1/Mult-Add Loop Carried Scalar Dependency

Sustained Interface Payload BW

Sustained GPIO Payload BW

OBM SRAM Size

GPIO Payload BW

DPFP Perf

SRC-6 Series E
SRC-7

• General Purpose computer system
• Evolution of SRC-6 product line
• Focus on higher bandwidth
  – Faster interconnect
  – More memory accesses
• Maintains software compatibility
Sustained Payload Bandwidths

- **μP to Hi-Bar®**
  - SRC-6: 1400 MB/s
  - SRC-7: 1400 MB/s

- **Hi-Bar® Switch**
  - (per Input or Output port)
  - SRC-6: 1400 MB/s

- **MAP Main I/O**
  - SRC-6: 2800 MB/s

- **MAP GPIO**
  - SRC-6: 4800 MB/s

- **MAP User Logic OBM**
  - SRC-6: 6400 MB/s
Sustained Payload Bandwidths

- **μP to Hi-Bar**
  - SRC-6: 157% 3600 MB/s
  - SRC-7: 3600 MB/s

- **Hi-Bar® Switch**
  - SRC-6: 157% 3600 MB/s
  - SRC-7: 3600 MB/s

- **MAP Main I/O**
  - SRC-6: 414% 14400 MB/s
  - SRC-7: 14400 MB/s

- **MAP GPIO**
  - SRC-6: 115% 10300 MB/s
  - SRC-7: 10300 MB/s

- **MAP User Logic OBM**
  - SRC-6: 275% 24000 MB/s
  - SRC-7: 24000 MB/s
MAP®
Series H Random Logic Variant

- 1 or 2 LVDS main I/O ports
- 150 MHz nominal User Logic speed
- OBM supports 20 simultaneous references
- 2 simultaneously accessible DDR2 SDRAM OBCM banks
- GPIO eXpansion (GPIOX) cards
- Streaming supported between I/O, OBCM, User Logic, OBM and GPIOX
GPIOX Cards

• Expansion cards fit inside 5.25” enclosure
  – The same cards are expected to work in all SRC form factors
    • 5.25”, Compact MAP™ and 6U

• SRC will develop high demand cards such as
  – OBMX: Expands OBM volume
    • Increases maximum number of simultaneous OBM accesses
  – IOX: User programmable LVDS or LVTTL I/O
    • Can be used to connect to a pair of switch ports
    • Connects to custom user hardware
  – OCX: Multiple OC interfaces
  – FCX: Multiple Fiber Channel interfaces
  – ADCX: Dual 10 bit 2 Gsample/s A/D converter

• Customers will be able to develop custom cards
  – Mechanical and electrical specs will be available
MAP®
Series H Floating Point Variant

14.4 GB/s sustained payload (7.2 GB/s per pair)

MAP

SDRAM 1 GB

Controller

User Logic 1

User Logic 1 30 Mgates

User Logic 2

User Logic 2 FP

Ten Banks On-Board Memory (80 MB SRAM)

SDRAM 1 GB

4.2 GB/s

24 GB/s (2.4 x 10)

16 GB/s

16.3 GB/s

10.3 GB/s

First Ever!
Reconfigurable Floating Point BLOCKS!

- Field Programmable Floating Point Device
- Hard floating point units with field programmable interconnect
- 56 DPFP mults and adders per chip
  - 34 Gflops
- 112 SPFP mults and adders per chip
  - 68 Gflops
- Each FP unit also performs 53 or 24 bit integer ops with 106 or 48 bit results
- Selectable 150 MHz or 300 MHz operation
MAPstation™ with 6 Port Hi-Bar™

- Two 4.2 GB/s Common Memory banks integrated into Hi-Bar
- Up to 3 MAPs (each with GPIOX & 2 CM banks) in single tower
- Single MAP systems do not require Hi-Bar, available in 2U
Hi-Bar sustains 3.6 GB/s payload per path with 180 ns latency per tier
2 tiers support 256 nodes
MAP can use 1 or 2 Hi-Bar ports
GPIO can be chained or used for direct data input to MAP
High Bandwidth Disk

- Sustained disk bandwidth equal to Hi-Bar port
- Up to 32 Tbytes with 10K random IOPs per assembly
- Accessible directly from MAP through the systems 64 bit virtual address space
- Controller will contain Complex DMA capability (scatter/gather, array merge, etc)
Carte SRC-7 Support

- Compatible Programming Model
- Continued full integration of tools
- Multi-clock rate support (150MHz, 300MHz)
- Functional Unit Adapt
- 10 or 20 Simultaneous OBM Bank References
- Multiple Input & Output Ports
- GPIOX Personalities
- Near Common Memory
- New Chip Types
- New 3rd Party Tools
- Global Resource Manager Enhancements
## SRC-7 Check List

<table>
<thead>
<tr>
<th>Feature</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Linux OS</td>
<td>✔️</td>
</tr>
<tr>
<td>Tightly Integrated Programming Environment</td>
<td>✔️</td>
</tr>
<tr>
<td>Standard (ANSI) High Level Language Programming</td>
<td>✔️</td>
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<tr>
<td>No Hardware Design Knowledge Required</td>
<td>✔️</td>
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<tr>
<td>Full Program Debug Environment</td>
<td>✔️</td>
</tr>
<tr>
<td>Highest Gate Count</td>
<td>✔️</td>
</tr>
<tr>
<td>High Bandwidth Interconnect</td>
<td>✔️</td>
</tr>
<tr>
<td>Reconfigurable Floating Point Blocks</td>
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<tr>
<td>High BW Mass Storage Accessible by ALL Processors</td>
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